|  |  |
| --- | --- |
|  | **DEPARTMENT OF COMPUTER ENGINEERING** |

**Experiment No. 06**

|  |  |
| --- | --- |
| Semester | S.E-Semester III – Computer Engineering |
| Subject | Digital Logic and Computer Architecture |
| Subject Professor In-charge | Prof. Avinash Shrivas |
| Assisting Teachers | Prof. Avinash Shrivas |

|  |
| --- |
| Student Name – Deep Salunkhe |
| Roll Number – 21102A0014 |
| Division and Batch – Division A, Batch 1 |
| Date of Implementation – 7/09/2022 |
| Experiment Title: To implement 4-bit ripple carry adder |
| **Theory:**  Ripple carry Adder  A ripple carry adder is **a digital circuit that produces the arithmetic sum of two binary numbers**. It. can be constructed with full adders connected in cascaded (see section 2.1), with the carry output. from each full adder connected to the carry input of the next full adder in the chain |
|  |

|  |
| --- |
| **Implementation**  **Ripple Carry adder**    Truth Table |
|  |